(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
14 June 2001 (14.06.2001)

PCT

(10) International Publication Number
WO 01/43181 A1

(51) International Patent Classification⁷: H01L 21/44, 21/48, 21/50, 23/06, 23/12, 23/53, 23/48, 23/52, 29/40

(21) International Application Number: PCT/IL00/00786

(22) International Filing Date:
26 November 2000 (26.11.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
133453 10 December 1999 (10.12.1999) IL

(71) Applicant *(for all designated States except US)*: SHELL-CASE LTD. [IL/IL]; P.O. Box 48328, Manhat Technology Park, 96251 Jerusalem (IL).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: BADEHI, Avner, Pierre [IL/IL]; 6 Nataf Street, 90804 Harei Yehuda (IL).

(74) Agents: COLB, Sanford, T. et al.; Sanford T. Colb & CO., P.O. Box 2273, 76122 Rehovot (IL).

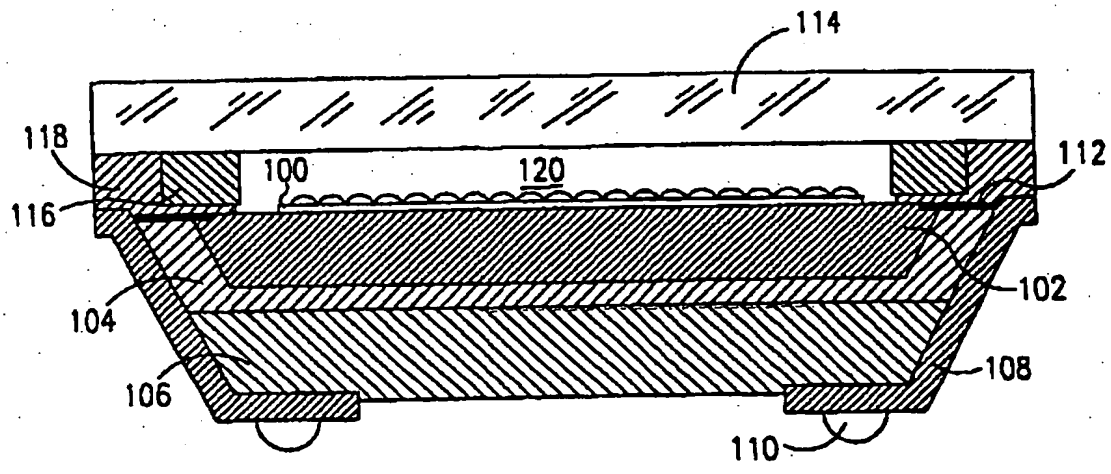
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*
— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHODS FOR PRODUCING PACKAGED INTEGRATED CIRCUIT DEVICES & PACKAGED INTEGRATED CIRCUIT DEVICES PRODUCED THEREBY



(57) Abstract: This invention discloses a crystalline substrate based device including a crystalline substrate (102) having formed thereon a microstructure (100); and at least one packaging layer (106) which is sealed over the microstructure by means of an adhesive and defines therewith at least one gap between the crystalline substrate (102) and the at least one packaging layer (106). A method of producing a crystalline substrate based device is also disclosed.

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METHODS FOR PRODUCING PACKAGED INTEGRATED CIRCUIT DEVICES & PACKAGED INTEGRATED CIRCUIT DEVICES PRODUCED THEREBY

FIELD OF THE INVENTION

The present invention relates to integrated circuits and similar devices generally and to methods for the manufacture thereof.

BACKGROUND OF THE INVENTION

An essential step in the manufacture of all integrated circuit devices is known as "packaging" and involves mechanical and environmental protection of a silicon chip which is at the heart of the integrated circuit as well as electrical interconnection between predetermined locations on the silicon chip and external electrical terminals.

At present three principal technologies are employed for packaging semiconductors: wire bonding, tape automatic bonding (TAB) and flip chip.

Wire bonding employs heat and ultrasonic energy to weld gold bonding wires between bond pads on the chip and contacts on the package.

Tape automatic bonding (TAB) employs a copper foil tape instead of bonding wire. The copper foil tape is configured for each specific die and package combination and includes a pattern of copper traces suited thereto. The individual leads may be connected individually or as a group to the various bond pads on the chip.

Flip chips are integrated circuit dies which have solder bumps formed on top of the bonding pads, thus allowing the die to be "flipped" circuit side down and directly soldered to a substrate. Wire bonds are not required and considerable savings in package spacing may be realized.

The above-described technologies each have certain limitations. Both wire bonding and TAB bonding are prone to bad bond formation and subject the die to relatively high temperatures and mechanical pressures. Both wire bond and TAB technologies are problematic from a package size viewpoint, producing integrated circuit devices having a die-to-package area ratio ranging from about 10% to 60%.

The flip-chip does not provide packaging but rather only interconnection. The interconnection encounters problems of uniformity in the solder bumps as well as in

thermal expansion mismatching, which limits the use of available substrates to silicon or materials which have thermal expansion characteristics similar to those of silicon.

The patent literature is extremely rich in the area of integrated circuits and methods for the manufacture thereof.

Described in applicant's published PCT Application WO 95/19645 are methods and apparatus for producing integrated circuit devices.

The following U.S. Patents and patent applications of the present inventor are considered to be particularly relevant: 5,716,759; 5,547,906; 5,455,455 and 08/952,019.

SUMMARY OF THE INVENTION

The present invention seeks to provide improved packaged crystalline substrate based devices and methods for producing same.

There is thus provided in accordance with a preferred embodiment of the present invention a crystalline substrate based device including a crystalline substrate having formed thereon a microstructure and at least one packaging layer which is sealed over the microstructure by an adhesive and defines therewith at least one gap between the crystalline substrate and the at least one packaging layer.

There is also provided in accordance with a preferred embodiment of the present invention a chip scale packaged crystalline substrate including:

a substrate having formed thereon a microstructure; and

at least one chip scale package which is sealed over the microstructure and defines therewith at least one gap.

There is additionally provided in accordance with a preferred embodiment of the present invention a method of producing a crystalline substrate based device including:

providing a microstructure on a substrate; and

adhesively sealing at least one packaging layer over the microstructure and at least partially spaced therefrom, thereby to define a gap between the microstructure and the at least one packaging layer.

Preferably, at least one packaging layer is sealed onto the crystalline substrate using an adhesive, such as epoxy.

In accordance with a preferred embodiment of the present invention, the crystalline substrate includes silicon, lithium niobate, lithium tantalate or quartz.

Preferably, the at least one packaging layer is transparent.

The at least one cavity may include a single cavity or a plurality of cavities.

The microstructure may include a micromechanical structure, a microelectronic structure and/or an optoelectronic structure.

BRIEF DESCRIPTION OF THE DRAWING

Figs. 1A and 1B are pictorial illustrations of a crystalline substrate based device having an internal cavity, constructed and operative in accordance with a preferred embodiment of the present invention;

Figs. 2A, 2B, 2C & 2D are simplified sectional illustrations of various crystalline substrate based devices constructed and operative in accordance with a preferred embodiment of the present invention, corresponding generally to Figs. 1A and 1B;

Fig. 3 is a partially cut-away sectional illustration of a crystalline substrate based device of the type shown in Figs. 1A & 1B;

Figs. 4A, 4B, 4C, 4D & 4E are simplified illustrations of steps in a method for producing a packaging layer for use in crystalline substrate based device in accordance with a preferred embodiment of the present invention;

Figs. 5A, 5B, 5C, 5D, 5E, 5F, 5G, 5H & 5I are simplified illustrations of steps in a method for producing a crystalline substrate based device of the type shown in Figs. 2A & 2C in accordance with a preferred embodiment of the present invention;

Figs. 6A, 6B, 6C, 6D, 6E, 6F, 6G, 6H, 6I, 6J & 6K are simplified illustrations of steps in a method for producing a crystalline substrate based device of the type shown in Fig. 2B in accordance with another preferred embodiment of the present invention;

Figs. 7A, 7B, 7C, 7D, 7E, 7F & 7G are simplified illustrations of steps in a method for producing a crystalline substrate based device of the type shown in Fig. 2D in accordance with another preferred embodiment of the present invention;

Figs. 8A and 8B are illustrations of apparatus typically employed in the manufacture of a crystalline substrate based devices of the type shown in Figs. 2A & 2C in the manner shown in Figs. 5A - 5I;

Figs. 9A and 9B are illustrations of apparatus typically employed in the manufacture of a crystalline substrate based devices of the type shown in Fig. 2B in the

manner shown in Figs. 6A - 6K; and

Figs. 10A and 10B are illustrations of apparatus typically employed in the manufacture of a crystalline substrate based devices of the type shown in Fig. 2D in the manner shown in Figs. 7A - 7G.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference is now made to Figs. 1A and 1B, which together illustrate a preferred embodiment of integrated circuit device constructed and operative in accordance with a preferred embodiment of the present invention. The integrated circuit device includes a relatively thin and compact, environmentally protected and mechanically strengthened integrated circuit package 10 having a multiplicity of electrical contacts 12 plated along the edge surfaces 14 thereof.

Preferably, contacts 12 extend over edge surfaces onto the planar surfaces 16 of the package. This contact arrangement permits both flat surface mounting and edge mounting of package 10 onto a circuit board. It is noted that the integrated circuit package 10 may include one or more of the following elements (not shown): an integrally formed dichroic filter, color filter, antireflective coating, polarizer, optical grating, integrated wave guide and optical coupling bumps.

In accordance with a preferred embodiment of the present invention, the integrated circuit package 10 defines a cavity 18, which is indicated in phantom lines.

Reference is now made to Figs. 2A - 2D, which illustrate four alternative preferred embodiments of integrated circuit devices of the general type shown in Figs. 1A & 1B, constructed and operative in accordance with another preferred embodiment of the present invention. Each of the devices shown in Figs. 2A - 2D includes a relatively thin and compact, environmentally protected and mechanically strengthened integrated circuit package having a multiplicity of electrical contacts plated along the edge surfaces thereof.

Fig. 2A shows an integrated circuit device including a microlens array 100 formed on a crystalline substrate 102. Underlying the substrate 102 and sealed thereto by epoxy 104 is a packaging layer 106, typically formed of glass, along edges of which are formed electrical contacts 108, typically defining bumps 110. Conductive pads 112 preferably connect substrate 102 to electrical contacts 108.

In accordance with a preferred embodiment of the present invention a packaging layer 114, typically formed of glass, and associated spacer elements 116, are sealed, by means of an adhesive such as epoxy 118, over substrate 102 so as to define a cavity 120 between the microlens array 100 and layer 114.

It is appreciated that packaging layer 114 is preferably transparent and may have formed thereon a dichroic filter and/or anti-reflective coating.

Fig. 2B shows an integrated circuit device including an optoelectronic or electromechanical device 150, such as a chemical sensor, a micromirror array or an accelerometer is suspended on a crystalline substrate 152, as by an electrically conductive connector 154. Sealed onto substrate 152 is a packaging layer 156 typically formed of glass, along edges of which are formed electrical contacts 158, typically defining bumps 160. Conductive pads 162 preferably connect substrate 152 to electrical contacts 158.

In accordance with a preferred embodiment of the present invention a packaging layer 164, typically formed of glass, and associated spacer elements 166, are sealed, by means of an adhesive, such as epoxy 168, over substrate 152 so as to define first and second cavities 170 and 172 between the device 150 and both layer 164 and layer 156.

It is appreciated that packaging layer 164 is preferably transparent and may have formed thereon a dichroic filter and/or anti-reflective coating.

Fig. 2C shows an integrated circuit device including a optoelectronic or electromechanical device 200 formed on a crystalline substrate 202. Underlying the substrate 202 and sealed thereto by epoxy 204 is a packaging layer 206, typically formed of glass, along edges of which are formed electrical contacts 208, typically defining bumps 210. Conductive pads 212 preferably connect substrate 202 to electrical contacts 208.

In accordance with a preferred embodiment of the present invention a packaging layer 214, typically formed of glass, and associated spacer elements 216, are sealed, by means of an adhesive such as epoxy 218, over substrate 202 so as to define a cavity 220 between the device 200 and layer 214.

It is appreciated that packaging layer 214 is preferably transparent and may have formed thereon a dichroic filter and/or anti-reflective coating.

Fig. 2D shows a Surface Acoustic Wave (SAW) device including a SAW

propagation surface 250 defined on a crystalline substrate 252, along edges of which are formed electrical contacts 258, typically defining bumps 260. Conductive pads 262 preferably connect substrate 252 to electrical contacts 258.

In accordance with a preferred embodiment of the present invention a packaging layer 264, typically formed of glass, and associated spacer elements 266, are sealed, by means of an adhesive such as epoxy 268, over substrate 252 so as to define a cavity 270 between surface 250 and layer 264.

Reference is now made to Fig. 3, which is a partially cut away illustration of a typical integrated circuit device of the type shown in Figs. 1A - 2D, having a cavity as indicated by reference numeral 280.

Reference is now made to Figs. 4A, 4B, 4C, 4D & 4E, which are simplified illustrations of steps in a method for producing a packaging layer for use in crystalline substrate based device in accordance with a preferred embodiment of the present invention. As seen in Figs. 4A & 4B, a substrate 300, typically formed of glass, is preferably coated with a layer 302 of epoxy based photoresist, typically SU-8 photoresist, commercially available from MicroChem Corp. of Newton, MA, USA.

The photoresist layer 302 is exposed via a mask 304, as shown in Fig. 4C and washed to define spacers 306 shown in Fig. 4D, which are typically of rectangular configuration, as indicated in Fig. 4E. These spacers correspond to spacer elements 116, 166, 216 and 266 in Figs. 2A - 2D respectively.

Reference is now made to Figs. 5A, 5B, 5C, 5D, 5E, 5F, 5G, 5H & 5I, which are simplified illustrations of steps in a method for producing a crystalline substrate based device of the type shown in Figs. 2A & 2C in accordance with a preferred embodiment of the present invention.

As seen in Fig. 5A, a packaging layer 400, typically of the type shown in Figs. 4D and 4E is provided. Adhesive 402 is applied thereto, preferably adjacent and between spacers 406 formed thereon, which correspond to the spacers 306 shown in Figs. 4D & 4E respectively and also correspond to spacer elements 116, 166, 216 and 266 in Figs. 2A - 2D respectively. Adhesive 402 is preferably a high temperature epoxy, such as EPO-TEK 353ND, commercially available from Epoxy Technology Inc. of Billerica, MA, USA.

As shown in Fig. 5B, the packaging layer 400, thus prepared, is adhered to a

crystalline substrate 404, typically having at least one metal layer thereon and having mounted thereon optomechanical or optoelectronic devices of the types described hereinabove with reference to Figs. 2A & 2C. As seen clearly, a cavity 405 is defined between the packaging layer 400 and the substrate 404, in accordance with a preferred embodiment of the present invention.

The crystalline substrate 404 is preferably lapped, as shown in Fig. 5C and etched, as shown in Fig. 5D, to define separate substrates 407. Following etching, the substrates 407 are adhered via an epoxy layer 408 to an underlying packaging layer 410, as shown in Fig. 5E.

As seen in Fig. 5F, the packaging layer 410 and epoxy layer 408 are mechanically notched and thereafter electrical contacts 412 and typically bumps 414 are formed thereon, as seen in Fig. 5G. The resulting assembly is diced as shown in Fig. 5H to yield a plurality of packaged integrated circuit devices, as seen in Fig. 5I.

It is appreciated that here and throughout all of the examples described herein, the crystalline substrate may be any suitable crystalline substrate and may comprise, for example, silicon, lithium niobate, lithium tantalate or quartz.

The manufacturing techniques described hereinabove and hereinbelow may but need not necessarily include techniques described in any of the following U.S. Patents and patent applications of the present inventor/assignee, the disclosure of which is hereby incorporated by reference: 5,716,759; 5,547,906; 5,455,455 and 08/952,019.

Reference is now made to Figs. 6A, 6B, 6C, 6D, 6E, 6F, 6G, 6H, 6I, 6J & 6K, which are simplified illustrations of steps in a method for producing a crystalline substrate based device of the type shown in Fig. 2B in accordance with another preferred embodiment of the present invention.

As seen in Fig. 6A, mounted on a substrate 500, typically formed of Pyrex are a plurality of crystalline substrates 502 onto which are formed pads 504 and onto which are suspended, as by electrically conductive connectors 506, optoelectronic or electromechanical devices 508, such as chemical sensors, micromirror arrays or an accelerometer, which may correspond to devices 150 of the type shown in Fig. 2B.

As shown in Fig. 6B, a packaging layer 510, typically of the type shown in Figs. 4D and 4E, is provided having adhesive 512 applied thereto, preferably adjacent and between spacers 516 formed thereon, which correspond to the spacers 306 shown in

Figs. 4D & 4E respectively and also correspond to spacer elements 116, 166, 216 and 266 in Figs. 2A - 2D respectively. Adhesive 512 is preferably a high temperature epoxy, such as EPO-TEK 353ND, commercially available from Epoxy Technology Inc. of Billerica, MA, USA.

As seen in Fig. 6C, the packaging layer 510, thus prepared, is adhered to crystalline substrates 502, typically adjacent pads 504. As seen clearly, a cavity 513 is defined between the packaging layer 510 and the substrates 502, and another cavity 514 is defined between substrates 502, substrate 500 and electromechanical devices 508 in accordance with a preferred embodiment of the present invention.

The substrate 500 and crystalline substrates 502 are preferably notched, as shown in Fig. 6D and etched, as shown in Fig. 6E, to define volumes 515 in crystalline substrates 502 which are preferably filled with epoxy 517, as shown in Fig. 6F.

As seen in Fig. 6G, the substrate 500, the epoxy 516 and the adhesive 512 are then mechanically notched to form a notch 501, and thereafter electrical contacts 519 are formed thereon, as by sputtering, as shown in Fig. 6H. Bumps 518 are formed thereon, as seen in Fig. 6I, preferably together with a NiAu coating. The resulting assembly is diced as shown in Fig. 6J to yield a plurality of packaged integrated circuit devices, as seen in Fig. 6K.

Reference is now made to Figs. 7A, 7B, 7C, 7D, 7E, 7F & 7G, which are simplified illustrations of steps in a method for producing a crystalline substrate based device of the type shown in Fig. 2D in accordance with another preferred embodiment of the present invention.

As seen in Fig. 7A, a packaging layer 600, typically of the type shown in Figs. 4D and 4E is provided. Adhesive 602 is applied thereto, preferably adjacent and between spacers 606 formed thereon, which correspond to the spacers 306 shown in Figs. 4D & 4E respectively and also correspond to spacer elements 116, 166, 216 and 266 in Figs. 2A - 2D respectively. Adhesive 602 is preferably a high temperature epoxy, such as EPO-TEK 353ND, commercially available from Epoxy Technology Inc. of Billerica, MA, USA.

As shown in Fig. 7B, the packaging layer 600, thus prepared, is adhered to a crystalline substrate 604, typically having at least one metal layer thereon and having defined thereon a SAW propagation layer 609 as described hereinabove with reference

to Fig. 2D. As seen clearly, a cavity 607 is defined between the packaging layer 600 and the SAW propagation layer 609, in accordance with a preferred embodiment of the present invention.

The crystalline substrate 604 can be lapped, as shown in Fig. 7C and notched partially into the adhesive 602, as shown in Fig. 7D, to define separate substrates 608. Following etching, electrical contacts 610 and typically bumps 614 are formed thereon, as seen in Fig. 7E. The resulting assembly is diced as shown in Fig. 7F to yield a plurality of packaged SAW devices, as seen in Fig. 7G.

Reference is now made to Figs. 8A and 8B, which are illustrations of apparatus employed in the manufacture of a crystalline substrate based devices of the type shown in Figs. 2A & 2C in the manner shown in Figs. 5A - 5I. As seen in Figs. 8A and 8B, a conventional wafer fabrication facility 680 provides complete wafers 681, of the type shown in Fig. 5A. Individual wafers 682 are bonded on their active surfaces to protective layers 683 as shown in Figs. 5A & 5B, by bonding apparatus 685, preferably having facilities for rotation of the wafer 682, the layer 683 and the epoxy so as to obtain even distribution of the epoxy.

The bonded wafer 686 is thinned (Fig. 5C) at its non-active surface as by grinding apparatus 684, such as Model 32BTGW using 12.5A abrasive 687, which is commercially available from Speedfam Machines Co. Ltd. of England.

The wafer is then etched (Fig. 5D) at its non-active surface, preferably by photolithography, such as by using conventional spin-coated photoresist, which is commercially available from Hoechst, under the brand designation AZ 4562, using a mask exposure machine 692 for the exposure of light sensitive photoresist 690 through the mask 691 and later etching the silicon in a bath 693 using solution 699.

The etched wafer 1000 is bonded (Fig. 5E) on the non-active side to protective layer 686 by bonding apparatus 694, which may be essentially the same as apparatus 685, to produce a doubly bonded wafer sandwich.

Notching apparatus 695 partially cuts the bonded wafer sandwich of Fig. 5E to the configuration shown in Fig. 5F.

The notched wafer 1002 is then preferably subjected to anti-corrosion treatment in a bath 696, containing a chromating solution 698, such as described in any of the following U.S. Patents: 2,507,956; 2,851,385 and 2,796,370, the disclosure of which is

hereby incorporated by reference.

Conductive layer deposition apparatus 700, which operates by vacuum deposition techniques, such as a Model 903M sputtering machine manufactured by Material Research Corporation of the U.S.A., is employed to produce a conductive layer on one or more surfaces of each die of the wafer as shown in Fig. 5G.

Configuration of contact strips, as shown in Fig. 5G, is carried out preferably by using conventional electro-deposited photoresist 701, which is commercially available from DuPont under the brand name Primecoat or from Shipley, under the brand name Eagle. The photoresist 701 is applied to the wafers 707 in a photoresist bath assembly 702, which is commercially available from DuPont or Shipley.

The photoresist 703 is preferably light configured by a UV exposure system 704, which may be identical to system 692, using a mask 705 to define suitable etching patterns. The photoresist is then developed in a development bath 706, and then the wafer is etched in a metal etch solution 708 located in an etching bath 710, thus providing a conductor configuration such as that shown in Fig. 5G.

The exposed conductive strips shown in Fig. 5G are then plated, preferably by electroless plating apparatus 712, which is commercially available from Okuno of Japan.

The wafer is then diced (Fig. 5H) into individual pre-packaged integrated circuit devices. Preferably the dicing blade 714 should be a diamond resinoid blade of thickness 4 - 12 mils. The resulting dies appear as illustrated generally in Fig. 5I.

Reference is now made to Figs. 9A and 9B, which are illustrations apparatus employed in the manufacture of a crystalline substrate based devices of the type shown in Fig. 2B in the manner shown in Figs. 6A - 6K. As seen in Figs. 9A and 9B, a wafer fabrication facility 780 provides complete wafers 781, of the type shown in Fig. 6A mounted onto a substrate, such as a Pyrex substrate 782. Individual wafers 781 are bonded on their active surfaces to protective layers 783 as shown in Figs. 6B & 6C, by bonding apparatus 784, preferably having facilities for rotation of the wafer 781, the layer 783 and the epoxy so as to obtain even distribution of the epoxy.

Notching apparatus 794 partially cuts the bonded wafer sandwich 793 of Fig. 6C to the configuration shown in Fig. 6D. The notched wafer 796 is then etched in a silicon etching solution 798 in a bath 1010. The etched voids 1012 in wafer 1014 are filled with

epoxy 1016, using a dispenser 1018 to fill the voids 1012, to obtain epoxy filled voids 1020. The wafer 1022 is notched again using apparatus 1024 through the epoxy filled trenches 1020.

The notched wafer 1028 is then preferably subjected to anti-corrosion treatment in a bath 1030, containing a chromating solution 1032, such as described in any of the following U.S. Patents: 2,507,956; 2,851,385 and 2,796,370, the disclosure of which is hereby incorporated by reference.

Conductive layer deposition apparatus 800, which operates by vacuum deposition techniques, such as a Model 903M sputtering machine manufactured by Material Research Corporation of the U.S.A., is employed to produce a conductive layer on one or more surfaces of each die of the wafer as shown in Fig. 6G.

Configuration of contact strips, as shown in Fig. 6E, is carried out preferably by using conventional electro-deposited photoresist 801, which is commercially available from DuPont under the brand name Primecoat or from Shipley, under the brand name Eagle. The photoresist is applied to the wafers 803 in a photoresist bath assembly 802, which is commercially available from DuPont or Shipley.

The photoresist 807 is preferably light configured by a UV exposure system 804 using a mask 805 to define suitable etching patterns. The photoresist is then developed in a development bath 806, and then etched in a metal etch solution 808 located in an etching bath 810, thus providing a conductor configuration such as that shown in Fig. 1B.

The exposed conductive strips shown in Fig. 6G are then plated, preferably by electroless plating apparatus 812, which is commercially available from Okuno of Japan.

The wafer is then diced (Fig. 6H) into individual pre-packaged integrated circuit devices. Preferably the dicing blade 814 should be a diamond resinoid blade of thickness 4 - 12 mils. The resulting dies appear as illustrated generally in Fig. 6K.

Reference is now made to Figs. 10A and 10B, which are illustrations apparatus employed in the manufacture of a crystal line substrate based device of the type shown in Fig. 2D in the manner shown in Figs. 7A - 7G. As seen in Figs. 10A and 10B, a conventional wafer fabrication facility 880 provides complete wafers 881, of the type shown in Fig. 7A. Individual wafers 881 are bonded on their active surfaces to

protective layers 883 as shown in Figs. 7A & 7B, by bonding apparatus 882, preferably having facilities for rotation of the wafer 881, the layer 883 and the epoxy so as to obtain even distribution of the epoxy.

Notching apparatus 894 partially cuts the wafer 883 of Fig. 7E to the configuration shown in Fig. 7F.

The notched wafer 884 is then preferably subjected to anti-corrosion treatment in a bath 896, containing a chromating solution 898, such as described in any of the following U.S. Patents: 2,507,956; 2,851,385 and 2,796,370, the disclosure of which is hereby incorporated by reference.

Conductive layer deposition apparatus 900, which operates by vacuum deposition techniques, such as a Model 903M sputtering machine manufactured by Material Research Corporation of the U.S.A., is employed to produce a conductive layer on one or more surfaces of each die of the wafer as shown in Fig. 7G.

Configuration of contact strips, as shown in Fig. 7E, is carried out preferably by using conventional electro-deposited photoresist 901, which is commercially available from DuPont under the brand name Primecoat or from Shipley, under the brand name Eagle. The photoresist 901 is applied to the wafers 903 in a photoresist bath assembly 902, which is commercially available from DuPont or Shipley.

The photoresist 920 is preferably light configured by a UV exposure system 904 using a mask 905 to define suitable etching patterns. The photoresist is then developed in a development bath 906, and then etched in a metal etch solution 908 located in an etching bath 910, thus providing a conductor configuration such as that shown in Fig. 1B.

The exposed conductive strips shown in Fig. 7G are then plated, preferably by electroless plating apparatus 912, which is commercially available from Okuno of Japan.

The wafer 913 is then diced (Fig. 5H) into individual pre-packaged integrated circuit devices. Preferably the dicing blade 914 should be a diamond resinoid blade of thickness 4 - 12 mils. The resulting dies appear as illustrated generally in Fig. 7G.

It will be appreciated by persons skilled in the art that the present invention is not limited by what has been particularly shown and described hereinabove. Rather the scope of the present invention includes both combinations and subcombinations of

various features described hereinabove as well as modifications and variations thereof which would occur to a person of skill in the art upon reading the foregoing description and referring to the drawings and which are not in the prior art.

CLAIMS

1. A crystalline substrate based device comprising:

a crystalline substrate having formed thereon a microstructure; and

at least one packaging layer which is sealed over said microstructure by means of an adhesive and defines therewith at least one gap between said crystalline substrate and said at least one packaging layer.

2. A crystalline substrate based device according to claim 1 and wherein said at least one packaging layer is sealed onto said crystalline substrate using an adhesive.

3. A crystalline substrate based device according to claim 2 and wherein said adhesive comprises epoxy.

4. A crystalline substrate based device according to claim 1 and wherein said crystalline substrate comprises silicon.

6. A crystalline substrate based device according to claim 1 and wherein said at least one packaging layer is transparent.

7. A crystalline substrate based device according to claim 1 and wherein said at least one cavity comprises a plurality of cavities.

8. A crystalline substrate based device according to claim 1 and wherein said microstructure comprises a micromechanical structure.

9. A crystalline substrate based device according to claim 1 and wherein said microstructure comprises a microelectronic structure.

10. A crystalline substrate based device according to claim 1 and wherein said microstructure comprises a optoelectronic structure.

11. A chip scale packaged crystalline substrate comprising:

a substrate having formed thereon a microstructure; and

at least one chip scale package which is sealed over said microstructure and defines therewith at least one gap.

12. A chip scale packaged crystalline substrate according to claim 11 and wherein said at least one package is sealed onto said substrate using an adhesive.

13. A chip scale packaged crystalline substrate based device according to claim 12 and wherein said adhesive comprises epoxy.

14. A chip scale packaged crystalline substrate according to claim 11 and wherein said substrate comprises silicon.

15. A chip scale packaged crystalline substrate according to claim 11 and wherein said substrate comprises lithium niobate.

16. A chip scale packaged crystalline substrate according to claim 11 and wherein said at least one package is at least partially transparent.

17. A chip scale packaged crystalline substrate according to claim 11 and wherein said at least one cavity comprises a plurality of cavities.

18. A chip scale packaged crystalline substrate according to claim 11 and wherein said microstructure comprises a micromechanical structure.

19. A chip scale packaged crystalline substrate according to claim 11 and wherein said microstructure comprises a microelectronic structure.

20. A chip scale packaged crystalline substrate according to claim 1 and wherein said microstructure comprises a optoelectronic structure.

21. A method of producing a crystalline substrate based device comprising:

providing a microstructure on a substrate; and

adhesively sealing at least one packaging layer over said microstructure and at least partially spaced therefrom, thereby to define a gap between said microstructure and said at least one packaging layer.

22. A method of producing a crystalline substrate based device according to claim 21 and wherein said at least one packaging layer is sealed onto said crystalline substrate using an adhesive.

23. A method of producing a crystalline substrate based device according to claim 22 and wherein said adhesive comprises Epoxy.

24. A method of producing a crystalline substrate based device according to claim 21 and wherein said crystalline substrate comprises silicon.

25. A method of producing a crystalline substrate based device according to claim 21 and wherein said crystalline substrate comprises lithium niobate.

26. A method of producing a crystalline substrate based device according to claim 21 and wherein said at least one packaging layer is transparent.

27. A method of producing a crystalline substrate based device according to claim 21 and wherein said at least one cavity comprises a plurality of cavities.

28. A method of producing a crystalline substrate based device according to claim 21 and wherein said microstructure comprises a micromechanical structure.

29. A method of producing a crystalline substrate based device according to claim 21 and wherein said microstructure comprises a microelectronic structure.

30. A method of producing a crystalline substrate based device according to claim 21 and wherein said microstructure comprises a optoelectronic structure.

31. A crystalline substrate based device according to claim 1 and wherein said crystalline substrate comprises lithium tantalate.

32. A crystalline substrate based device according to claim 1 and wherein said microstructure comprises a surface acoustic wave device.

33. A chip scale packaged crystalline substrate according to claim 1 and wherein said microstructure comprises a surface acoustic wave device.

34. A method of producing a crystalline substrate based device according to claim 21 and wherein said crystalline substrate comprises lithium tantalate.

35. A method of producing a crystalline substrate based device according to claim 21 and wherein said microstructure comprises a surface acoustic wave device.

36. A crystalline substrate based device according to claim 1 and wherein said crystalline substrate comprises quartz.

37. A method of producing a crystalline substrate based device according to claim 21 and wherein said crystalline substrate comprises quartz.

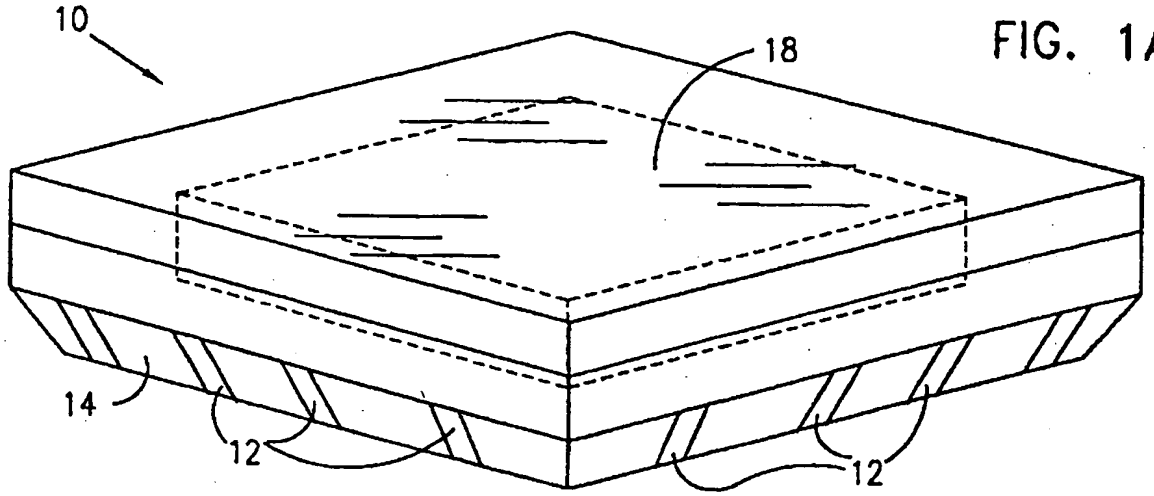


FIG. 1A

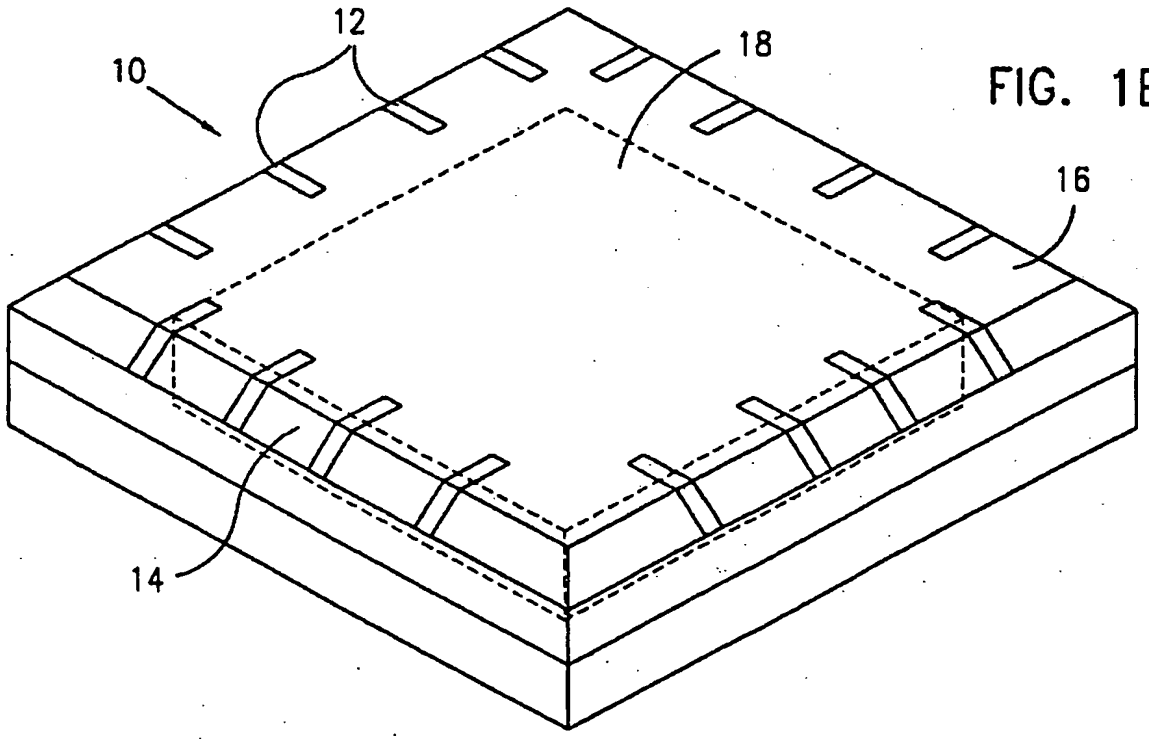


FIG. 1B

FIG. 2A

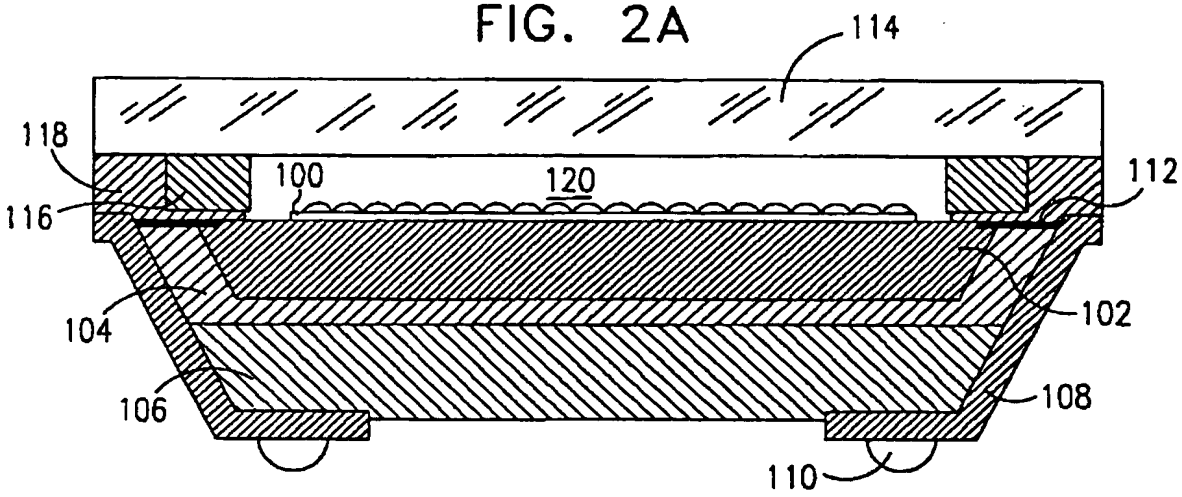


FIG. 2B

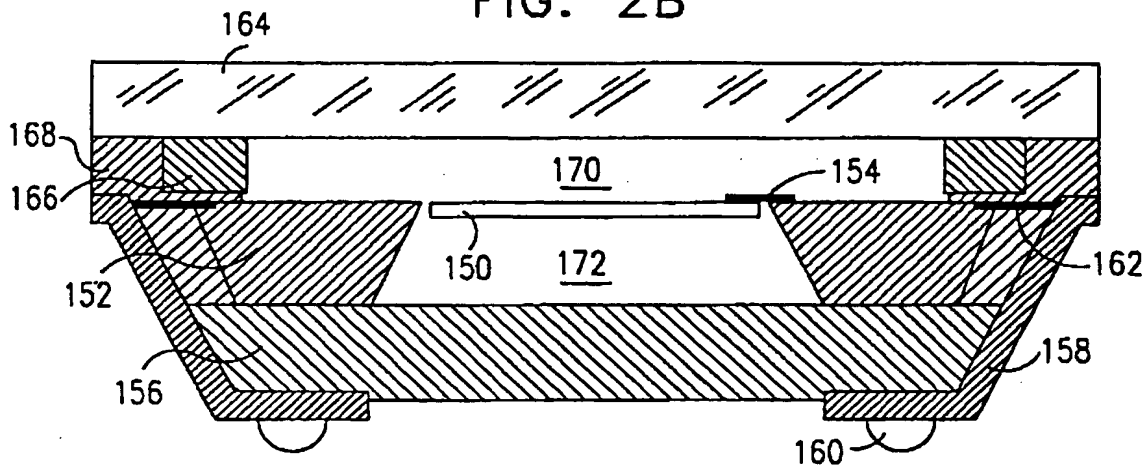


FIG. 2C

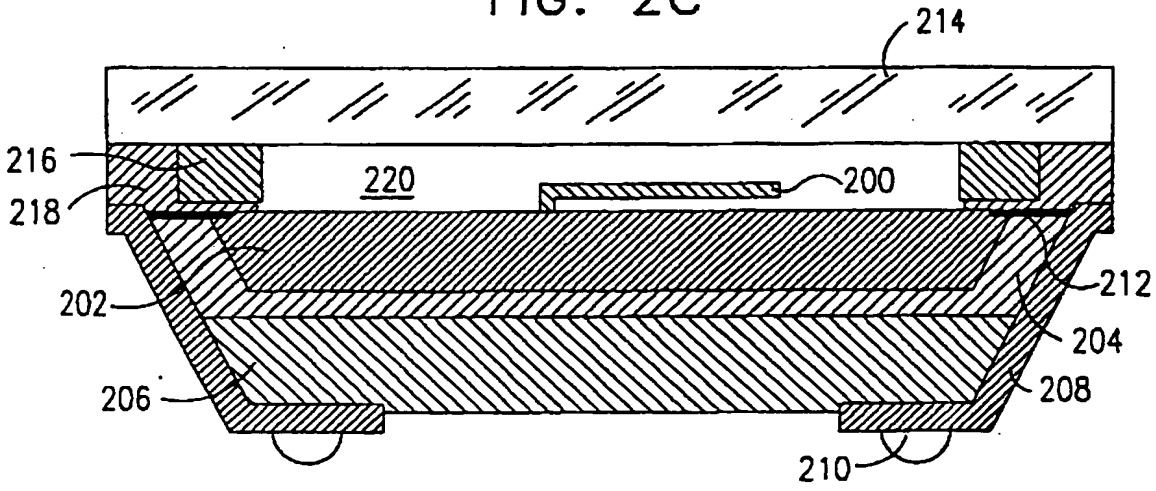


FIG. 2D

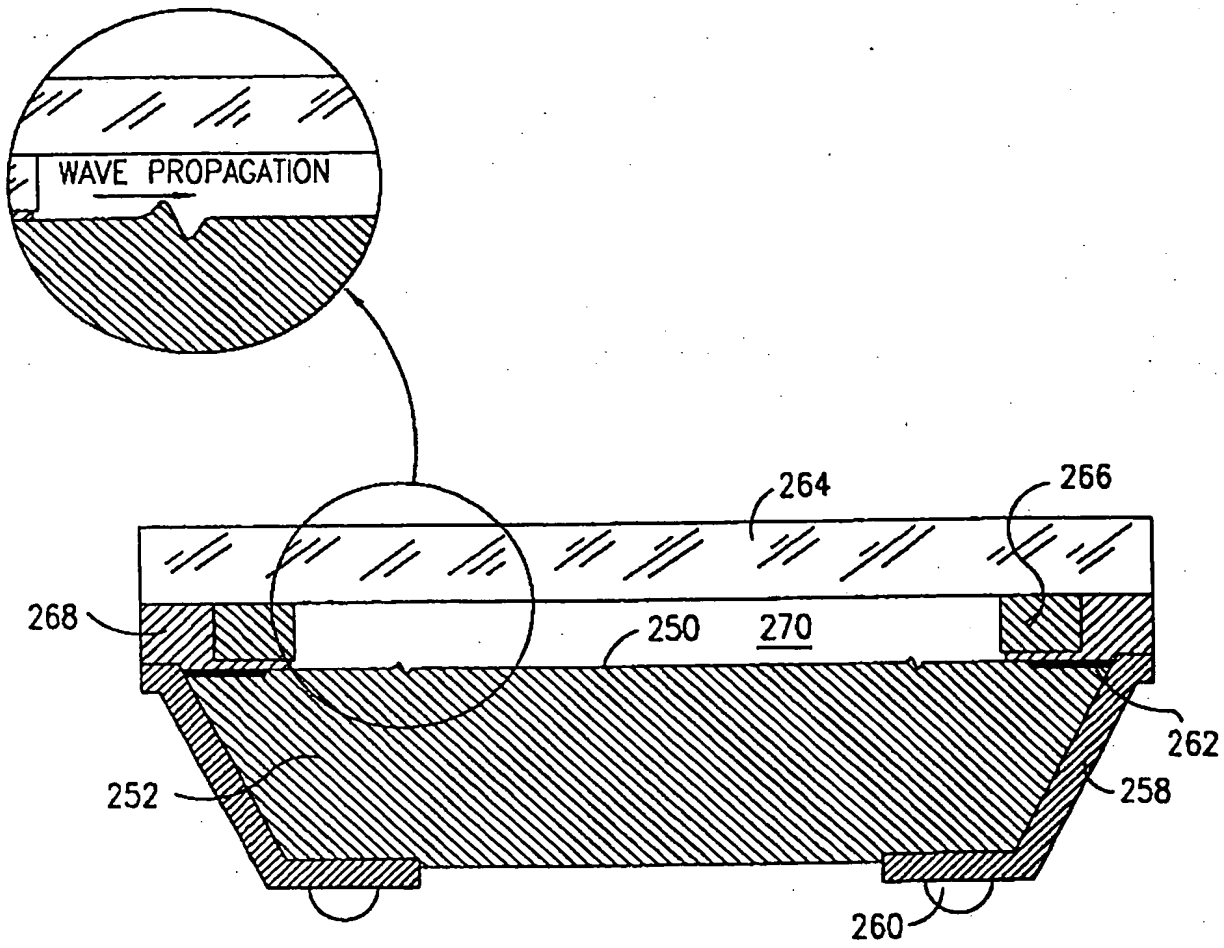


FIG. 3

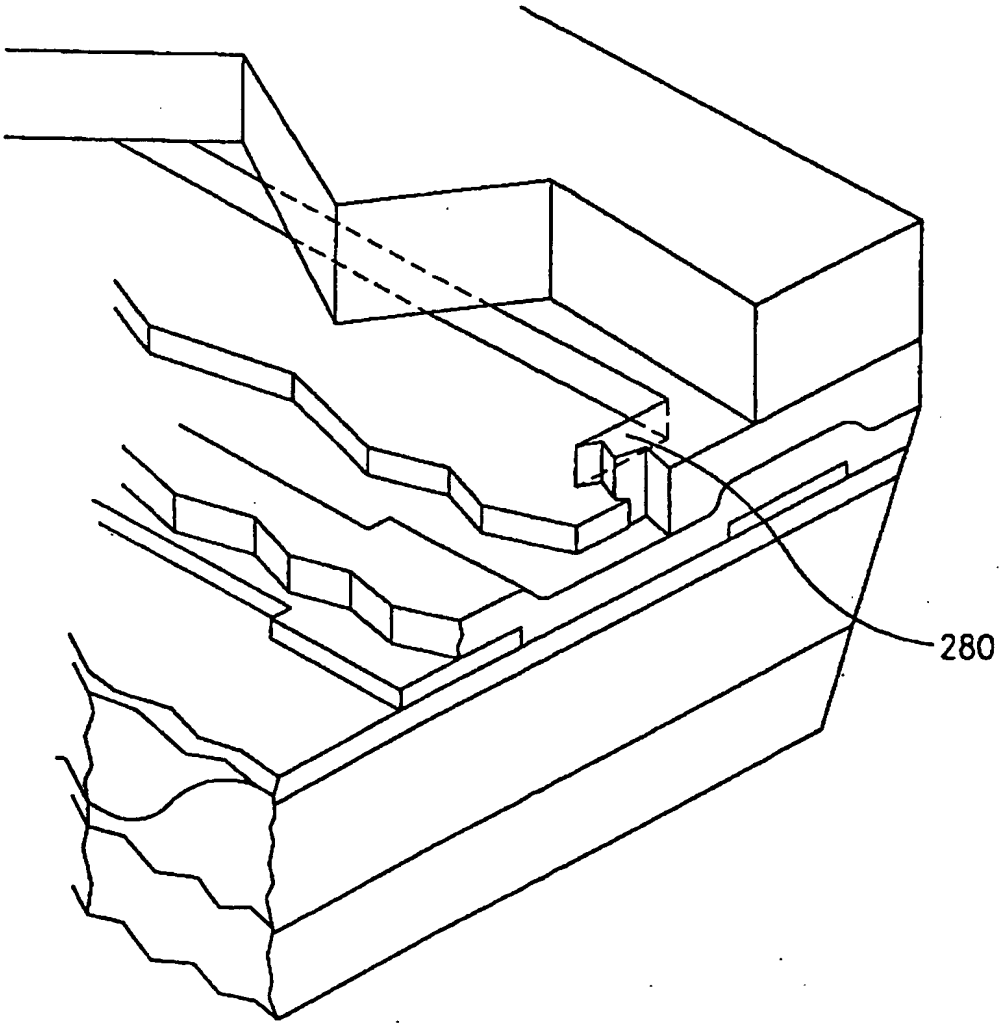


FIG. 4A

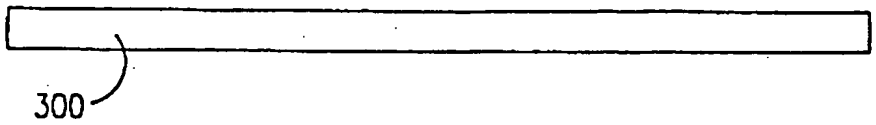


FIG. 4B

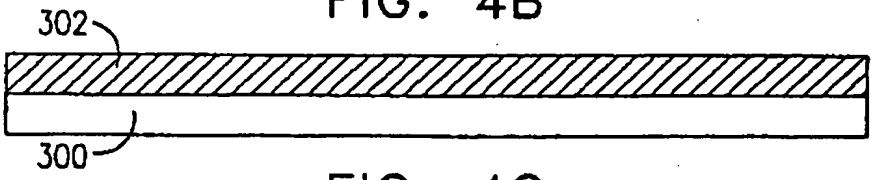


FIG. 4C

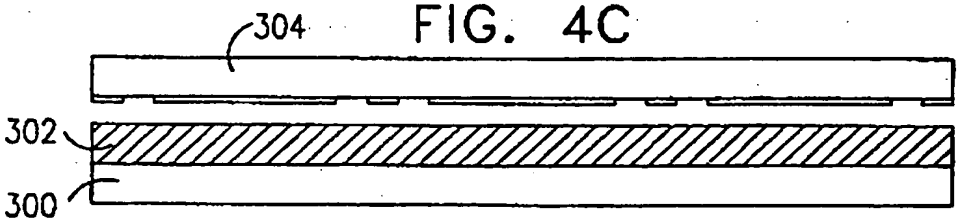


FIG. 4D

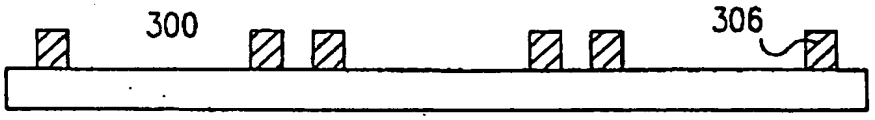


FIG. 4E

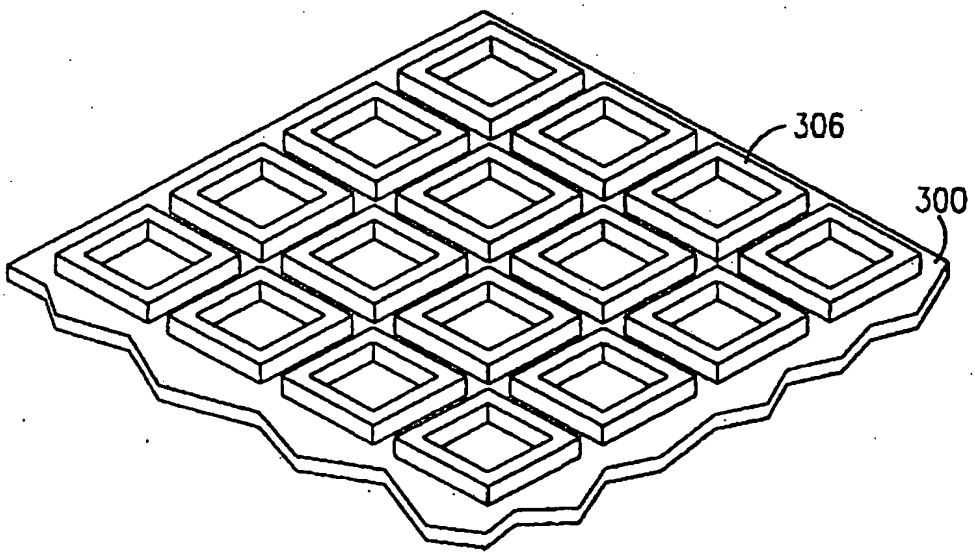


FIG. 5A

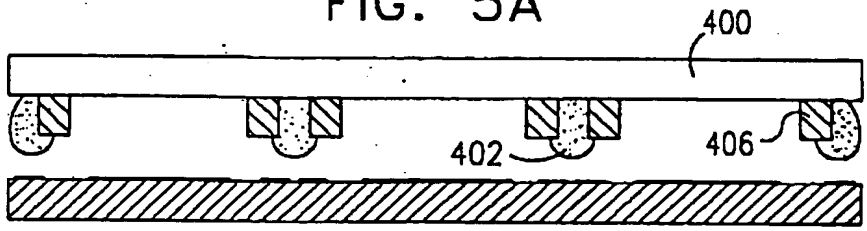


FIG. 5B

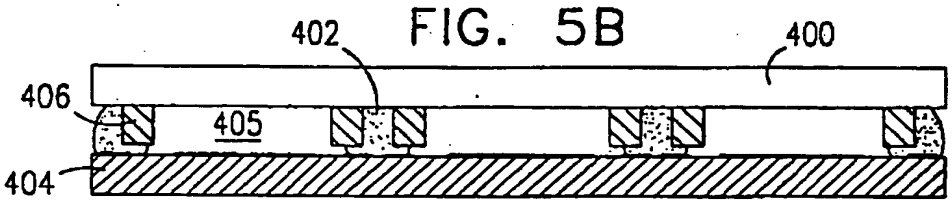


FIG. 5C

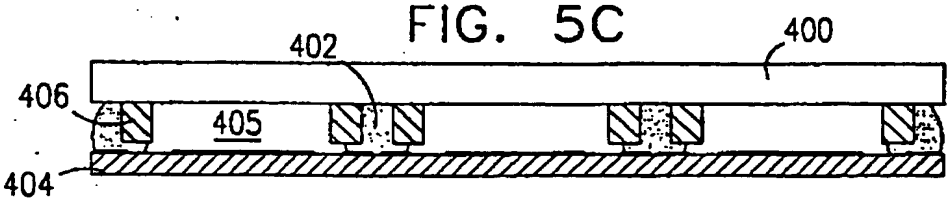


FIG. 5D

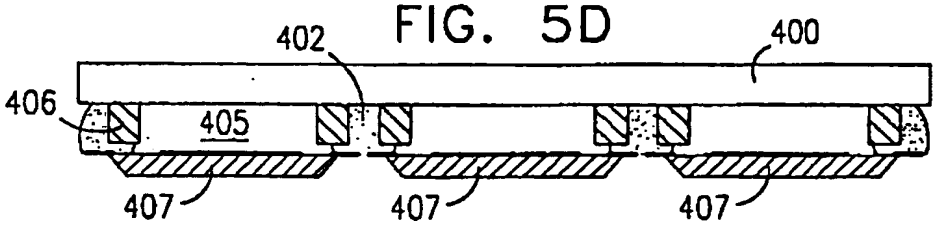


FIG. 5E

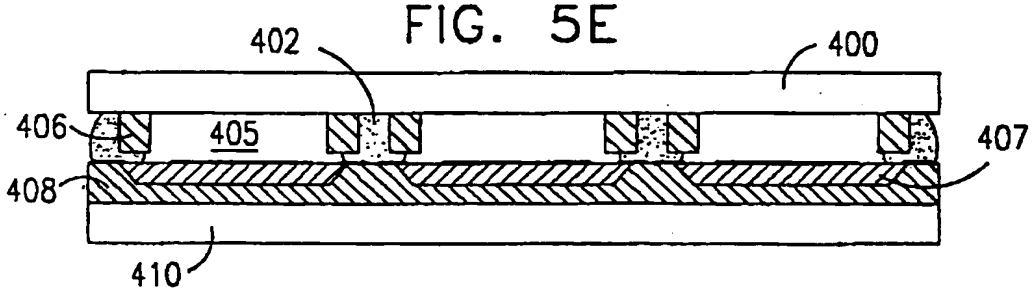


FIG. 5F

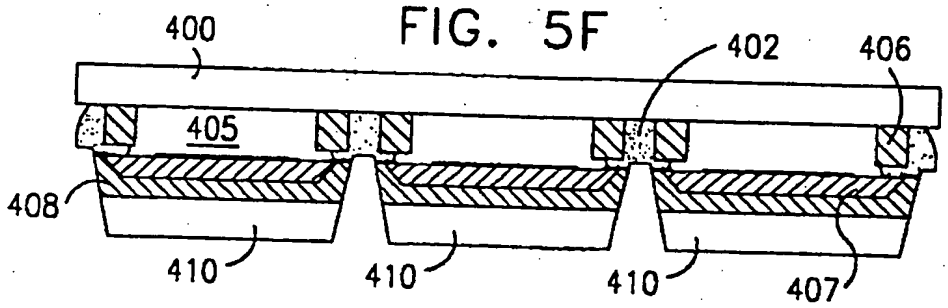


FIG. 5G

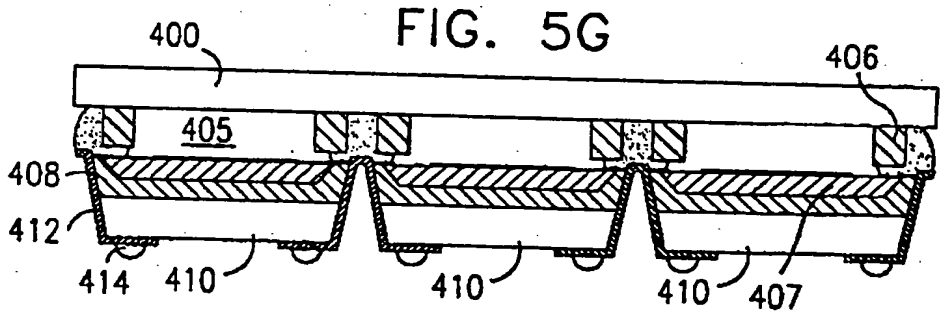


FIG. 5H

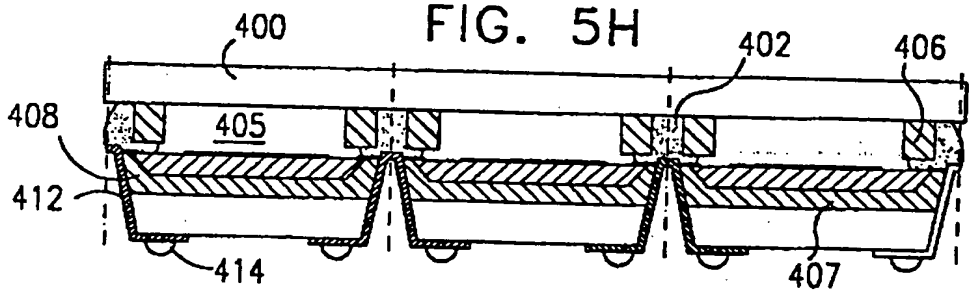


FIG. 5I

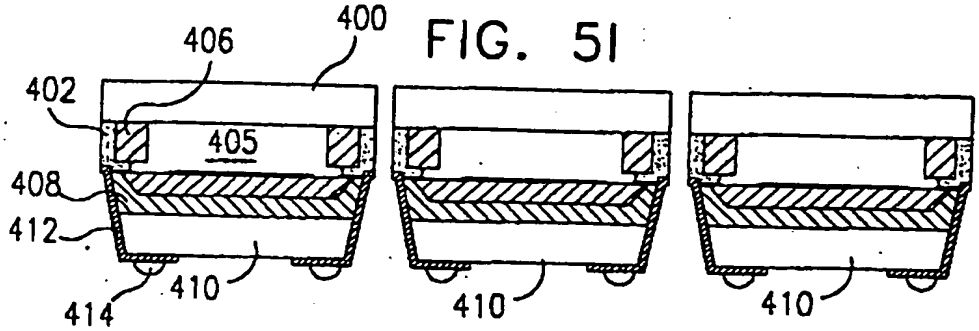


FIG. 6A

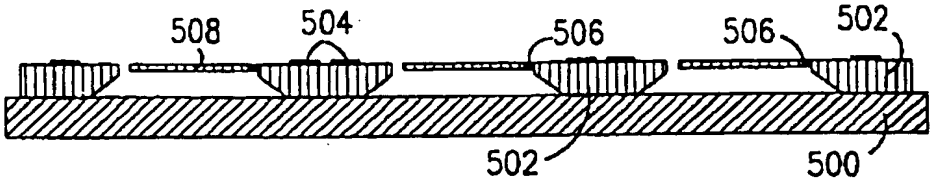


FIG. 6B

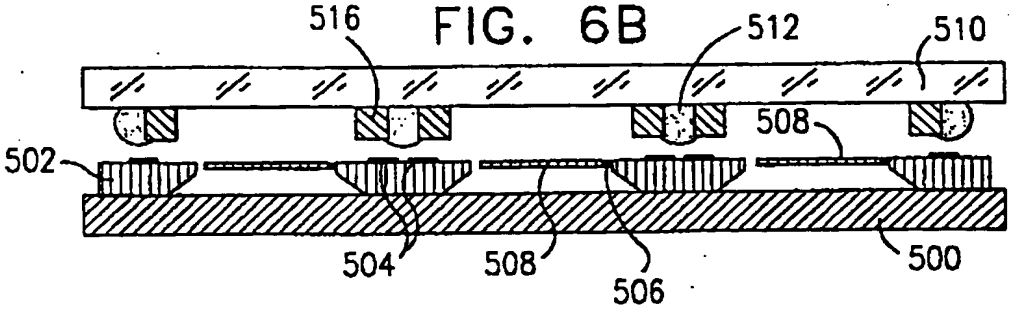


FIG. 6C

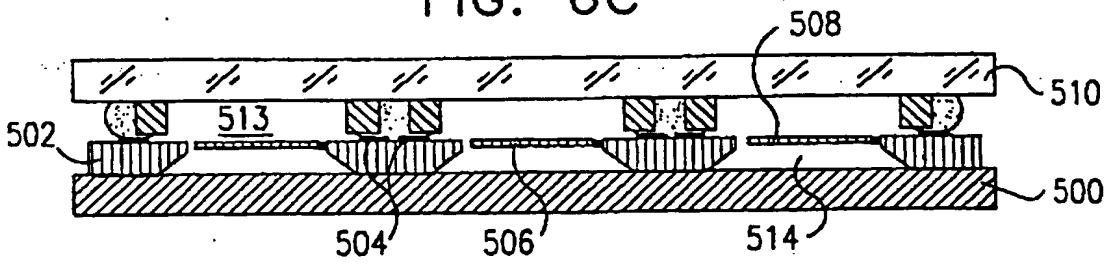


FIG. 6D

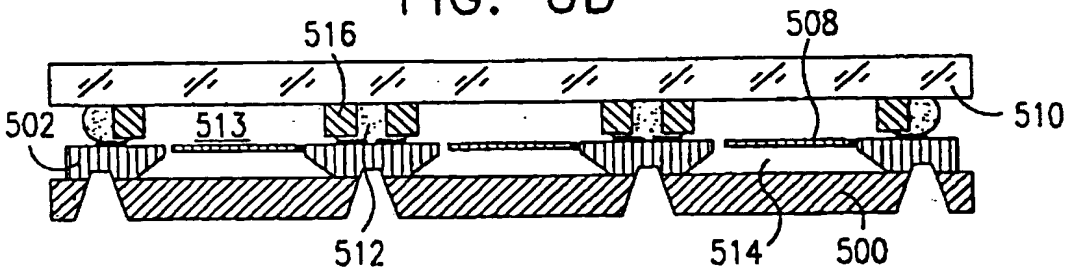


FIG. 6E

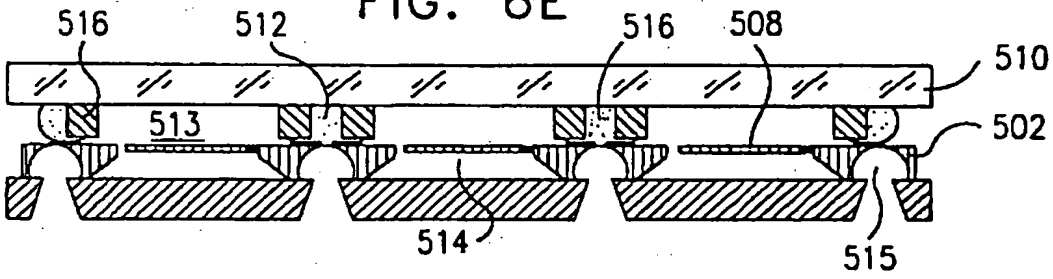


FIG. 6F

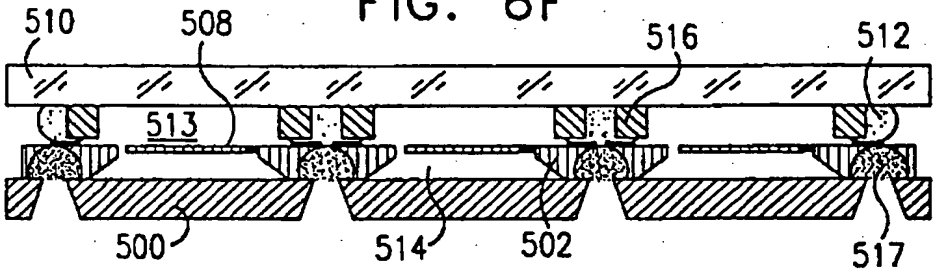


FIG. 6G

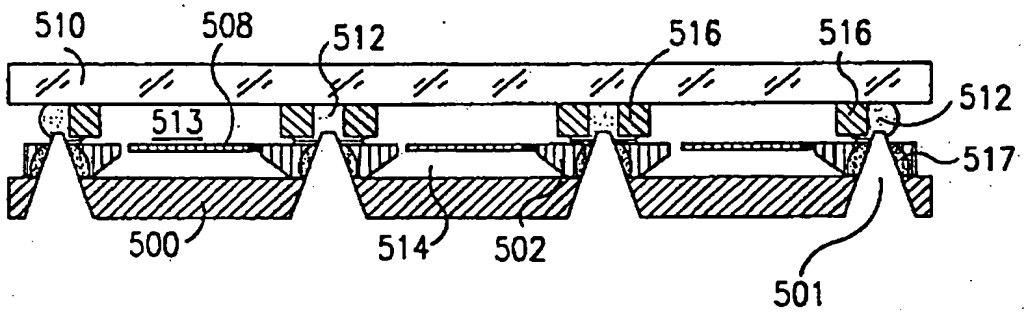


FIG. 6H

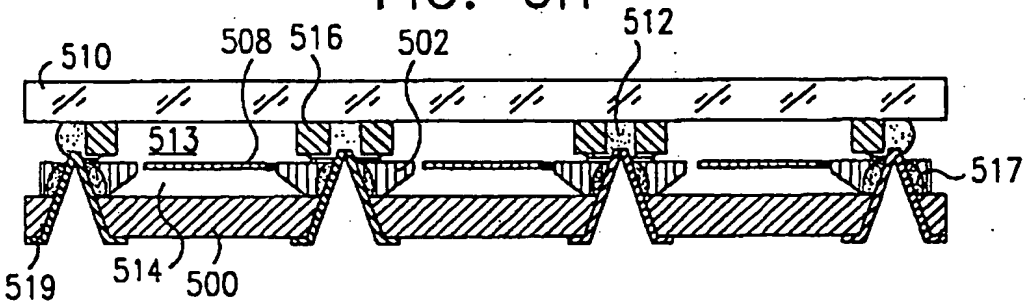


FIG. 6I

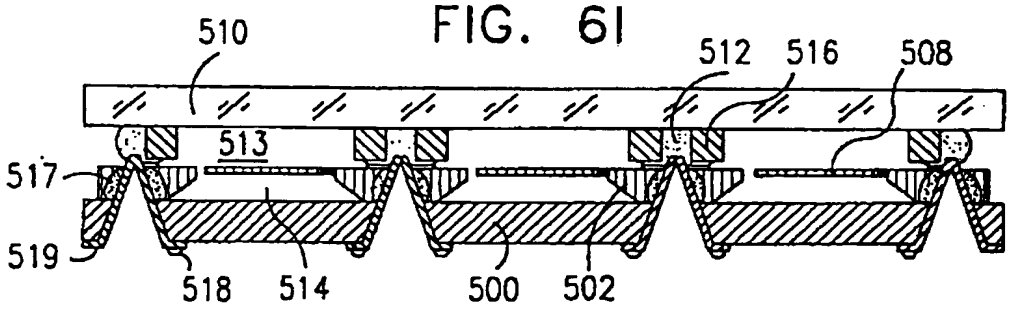


FIG. 6J

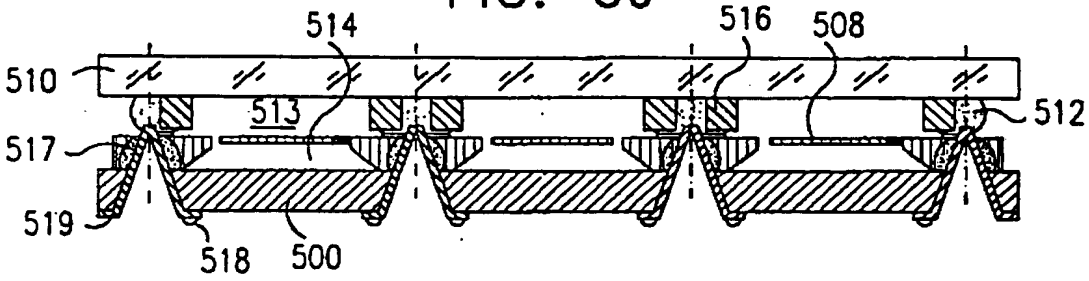


FIG. 6K

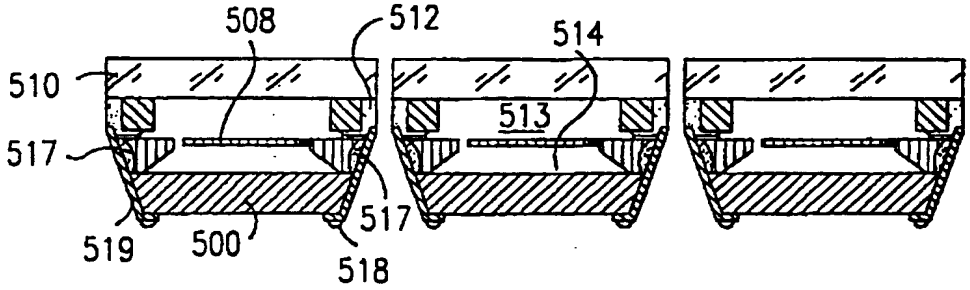


FIG. 7A

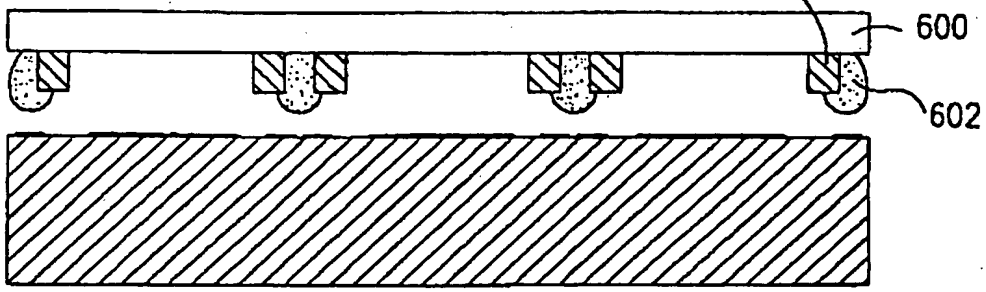


FIG. 7B

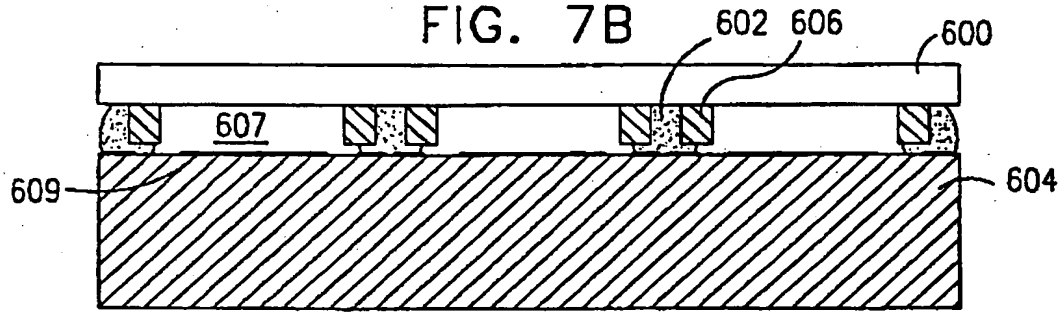


FIG. 7C

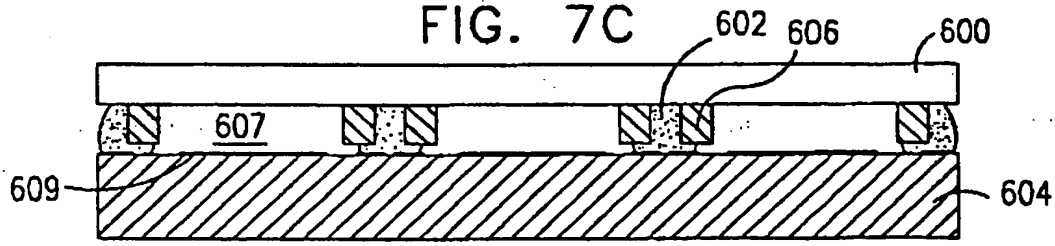


FIG. 7D

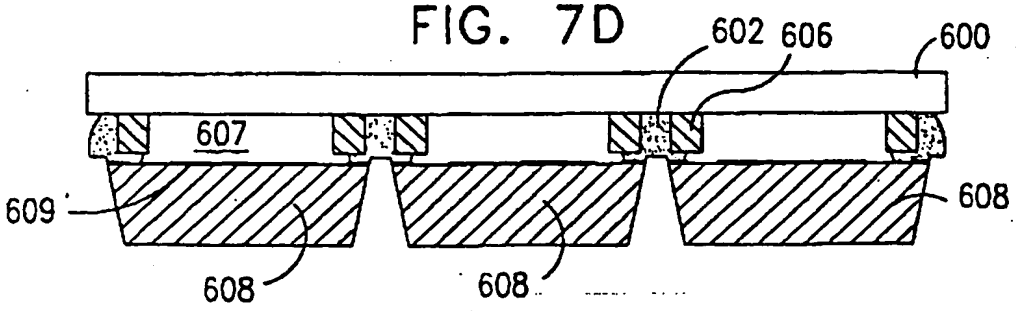


FIG. 7E

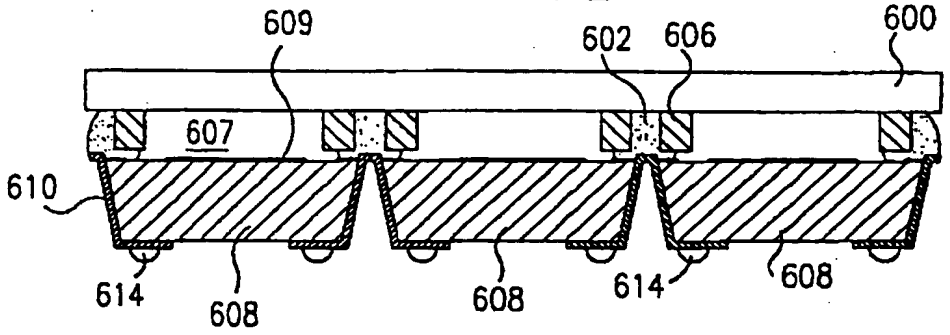


FIG. 7F

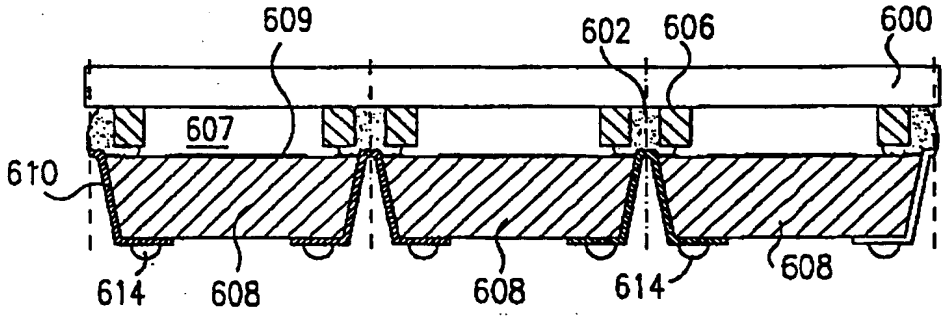
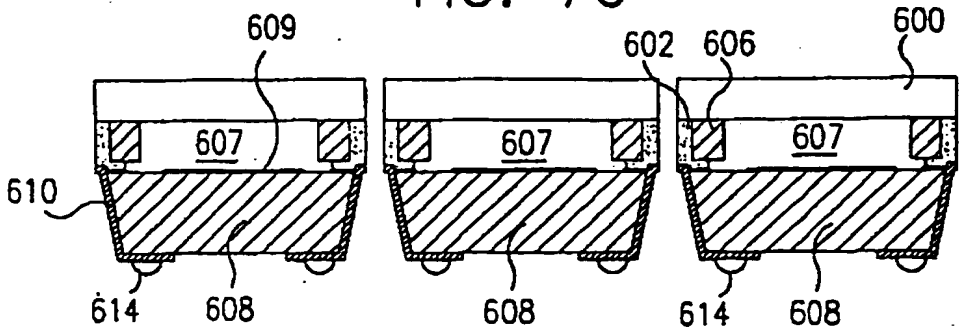


FIG. 7G



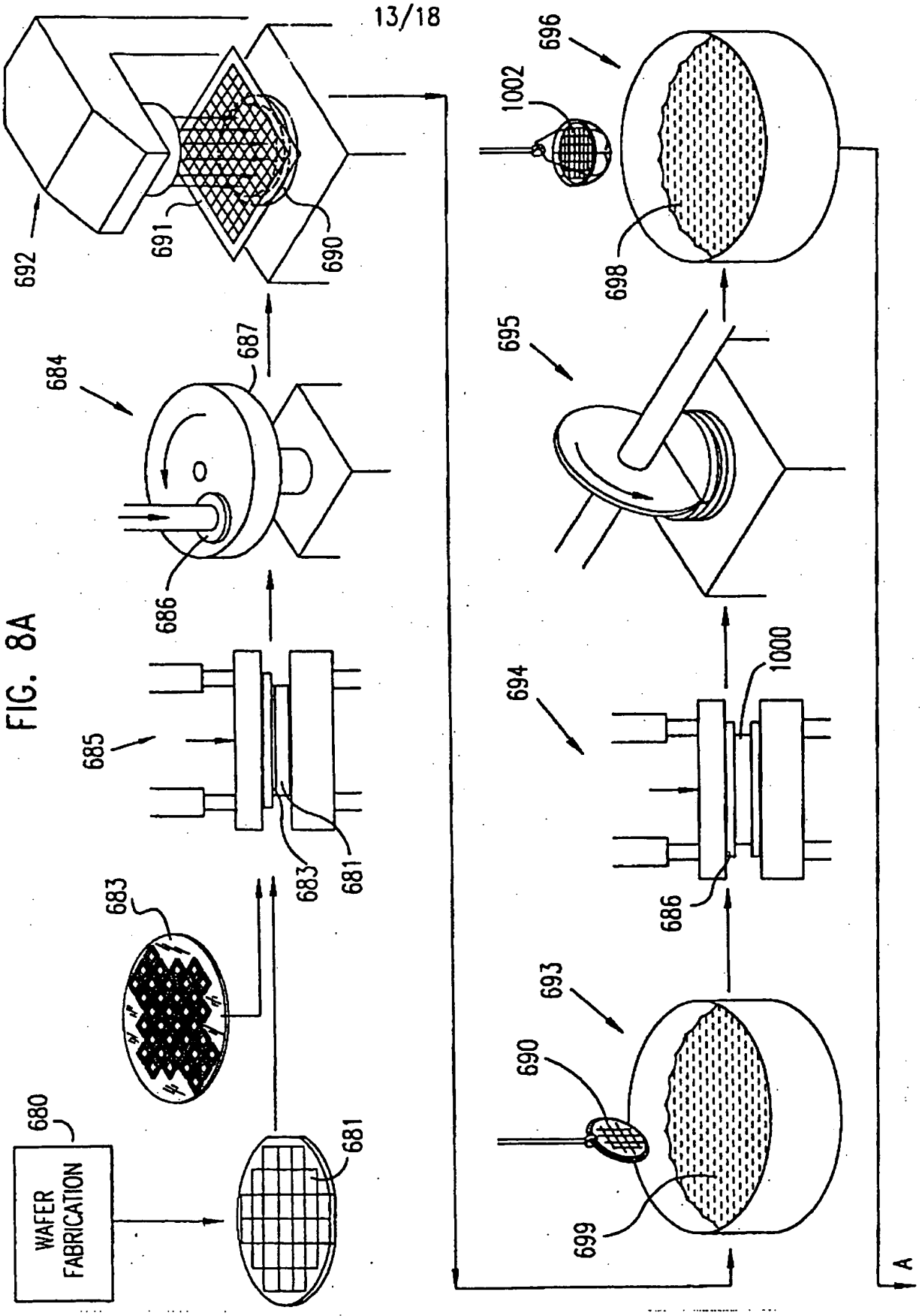

WAFER FABRICATION
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FIG. 8A

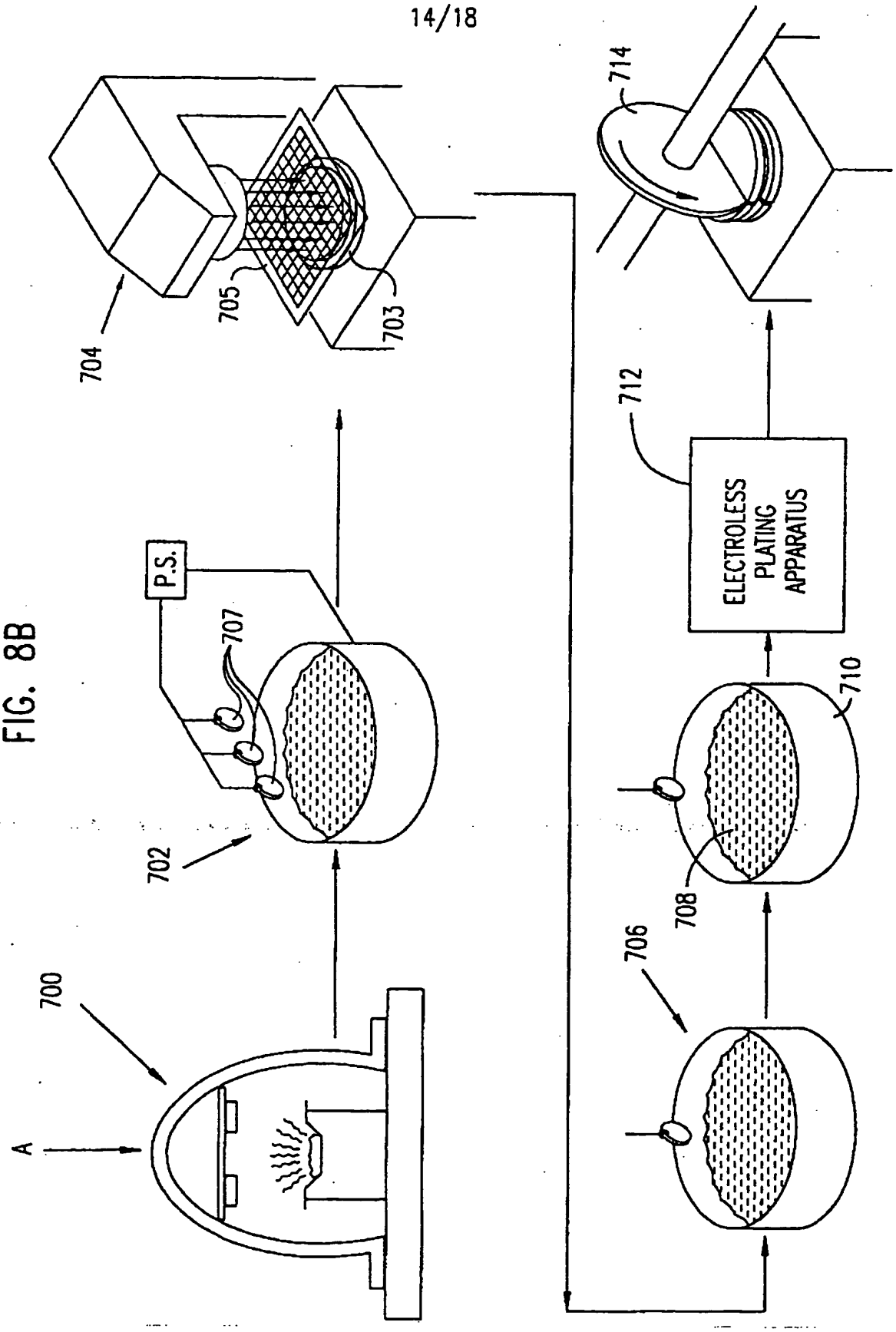
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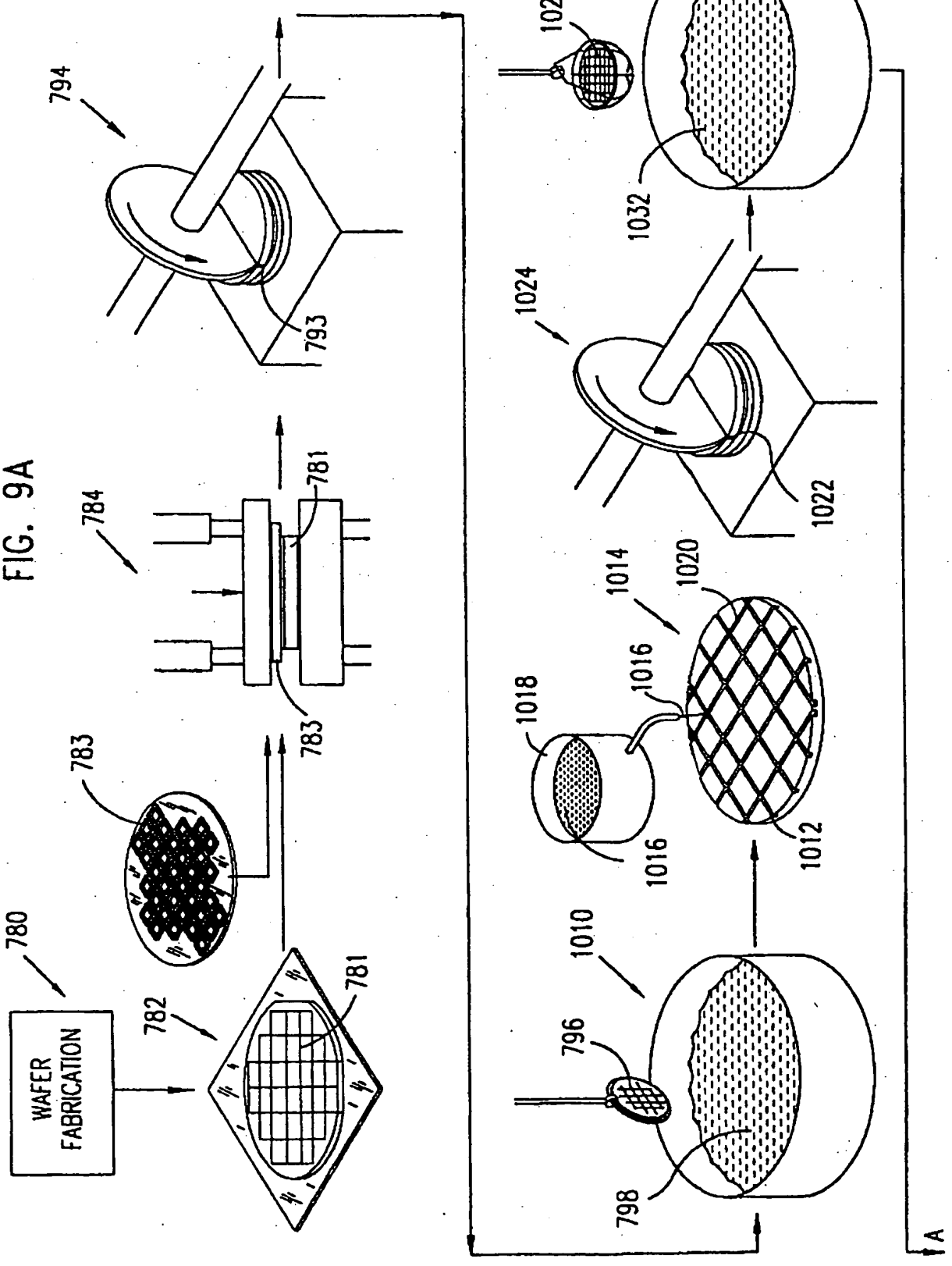
FIG. 8B

FIG. 9A


WAFER FABRICATION
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794
793
796
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1014
1016
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1024
1028
1030
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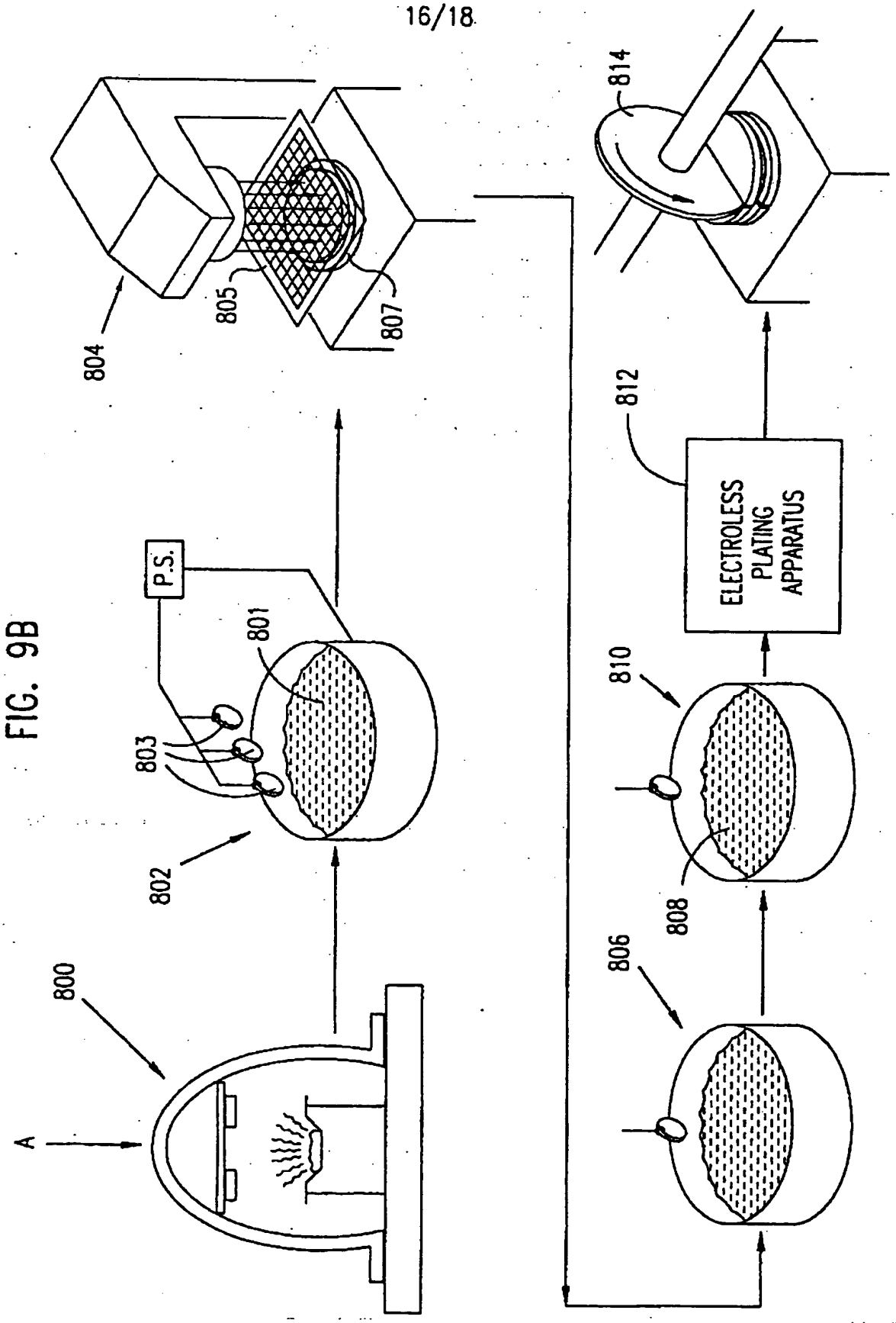
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ELECTROLESS PLATING APPARATUS
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FIG. 9B

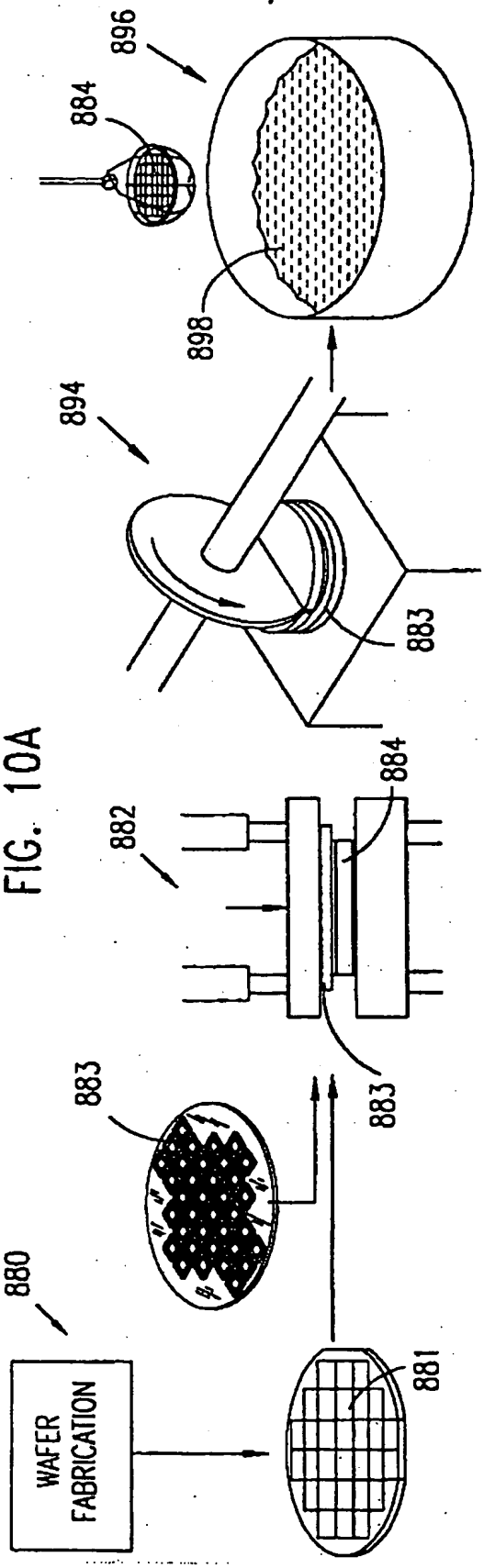
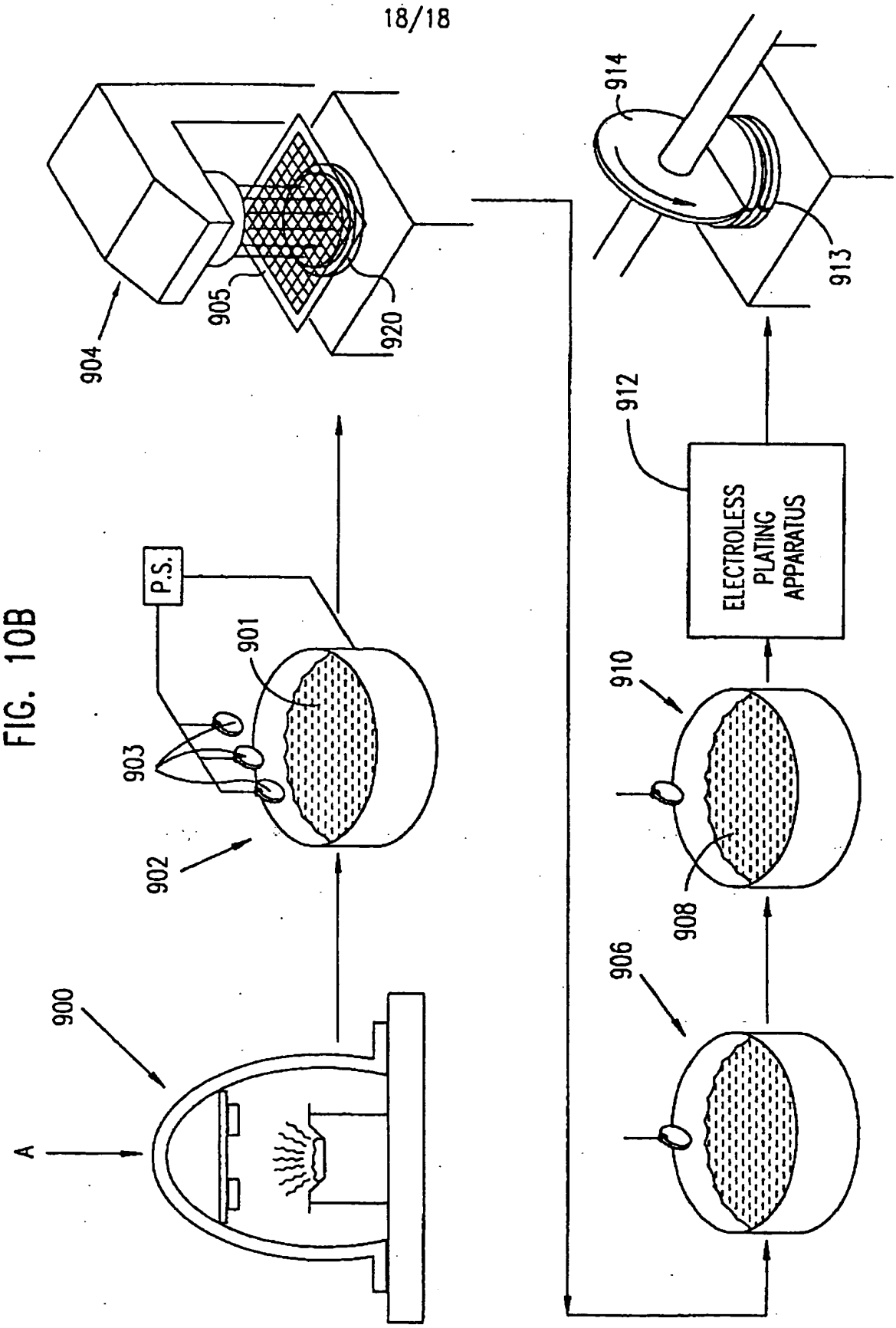


FIG. 10A

FIG. 10B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INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL00/00786

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) :H01L 21/44, 48, 50; 23/ 06, 12, 53, 48, 52; 29/40
US CL :438/110, 118; 257/701, 749, 750, 753
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/110, 118; 257/701, 749, 750, 753

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

BRS East
search terms: crystalline substrate, package

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,719,979 A (FURUYAMA) 17 February 1998 (17.02.1998), col. 7, lines 66-67; col. 8, lines 1-5, 13-30; col. 12, lines 11-49	1-4, 6, 9-10, 11-14, 16, 19-20, 21-24, 26, 29-30
Y	US 4,943,844 A (OSCILOWSKI et al.) 24 July 1990 (24.07.1990), col. 3, lines 1-68; col. 4, lines 1-68.	6-8, 16-18, 26-28
Y	US 4,633,573 A (SCHERER) 06 January 1987 (06.01.1987), col. 4, lines 32-68; col. 5, lines 1-68; col. 6, 1-68; col. 7, lines 1-50.	1-4 and 6-37
A	US 4,908,086 A (GOODRICH et al.) 13 March 1990 (13.03.1990), see entire document.	1-4 and 6-37

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principl- or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
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Date of the actual completion of the international search 15 MARCH 2001	Date of mailing of the international search report 04 MAY 2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer Sharon D. Hoppe JOHN NIEBLING Telephone No. (703) 308-3325

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